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Amendments to the Claims:

This listing of the claims will replace all prior versions, and listings, of the claims in the application.

Listing of the Claims:

Claims 1-2 (canceled)

Claim 3 (currently amended): The system of claim ~~1~~ 19

wherein the sequential readout circuit determines a difference between a final integration light value and a reset value for each photocell in a time sequential manner.

Claim 4 (currently amended): The system of claim ~~1~~ 19 wherein the array includes a plurality of columns; wherein the system further includes

a sample and hold circuit for each column; wherein each sample and hold circuit samples and holds ~~the~~ a voltage value of a photocell that is disposed in the respective column; wherein each sample and hold circuit includes

a single sampling capacitor, and

a single transistor coupled to the single sampling capacitor.

Claim 5 (currently amended): The system of claim ~~1~~ 19 ~~wherein the sequential readout circuit includes an amplifier that includes a first input; an output; and~~ further comprising:

an integration capacitor having a first electrode for coupling to the ~~first~~ input of the single amplifier and a second electrode for coupling to the output of the single amplifier; wherein the single amplifier includes a charge transfer mode and a unity gain mode.

Claim 6 (currently amended): The system of claim ~~1~~ 19 wherein the sequential readout circuit includes

a level shifting circuit coupled to the ~~first~~ input and the output of the single amplifier for performing level shifting of the output of the single amplifier.

Claim 7 (currently amended): The system of claim ~~1~~ 19 wherein the sequential readout circuit includes

a gain manipulation circuit coupled to the ~~first~~ input and the output of the single amplifier for performing gain manipulation of the single amplifier.

Claim 8 (currently amended): The system of claim ~~1~~ 19 wherein each photocell includes

a photodiode for detecting light and responsive thereto for generating a voltage representation thereof; wherein the photodiode includes an integration node;

a first transistor coupled to the photodiode for resetting the integration node in response to a reset signal;

a second transistor coupled to the integration node for shifting the level of the voltage at the integration node; and

a third transistor coupled to the second transistor for reading out the level-shifted voltage in response to a read signal.

Claim 9 (currently amended): The system of claim ~~1~~ 19 wherein the system is implemented in one of a scanner application, an optical mouse application, a video game controller application, a movement encoder application, a near field application, and a far field application.

Claim 10 (currently amended): A sequential readout circuit for coupling to an array of photocells; wherein the array includes at least a first row, a first column, a second column, a first photocell that is disposed in the first row and the first column, and a second photocell that is disposed in the first row and in the second column, the sequential readout circuit comprising:

a) ~~an~~ a single amplifier for reading out ~~the~~ a value of the photocells in the array one photocell at a time;

b) a first switch for selectively coupling the amplifier to the first column; and

c) a second switch for selectively coupling the amplifier to the second column.

Claim 11 (original): The sequential readout circuit of claim 10 wherein the single amplifier determines the difference between a reset voltage (V_{reset}) and a light voltage (V_{light}) for the first photocell and the second photocell in a time sequential manner.

Claim 12 (original): The sequential readout circuit of claim 10 further comprising:

a sample and hold circuit for each column; wherein each sample and hold circuit samples and holds the voltage value of a photocell that is disposed in the respective column.

Claim 13 (currently amended): The sequential readout circuit of claim 12 wherein each sample and hold circuit includes

a sampling capacitor, and

a transistor coupled to the ~~first~~ sampling capacitor.

Claim 14 (original): The sequential readout circuit of claim 10

wherein the amplifier includes a charge transfer mode, a unity gain mode, a first input; and an output; and

wherein the circuit further includes an integration capacitor having a first electrode for coupling to the first input and a second electrode for coupling to the output of the amplifier.

Claim 15 (original): The sequential readout circuit of claim 10 further comprising:

a level-shifting mechanism coupled to the amplifier for performing level shifting of the output of the amplifier.

Claim 16 (original): The sequential readout circuit of claim 10 further comprising:

a gain mechanism coupled to the amplifier for performing gain manipulation of the amplifier.

Claim 17 (original): The sequential readout circuit of claim 10 wherein each photocell includes

a photodiode for detecting light and responsive thereto for generating a voltage representation thereof; wherein the photodiode includes an integration node;

a first transistor coupled to the photodiode for resetting the integration node in response to a reset signal;

a second transistor coupled to the integration node for shifting the level of the voltage at the integration node; and

a third transistor coupled to the second transistor for reading out the level-shifted voltage in response to a read signal.

Claim 18 (original): The sequential readout circuit of claim 10 wherein the sequential readout circuit is implemented in one of a scanner application, an optical mouse application, a video game controller application, a movement encoder application, a near field application, and a far field application.

Claim 19 (new): A system comprising:

a) an array of photocells that are arranged in rows and columns; and

b) a sequential readout circuit for sequentially reading out the value of the photocells one photocell at a time; wherein the sequential readout circuit includes a single amplifier that includes an input for coupling to one column of the array of photocells at a time and an output for generating a voltage value corresponding to a photocell.